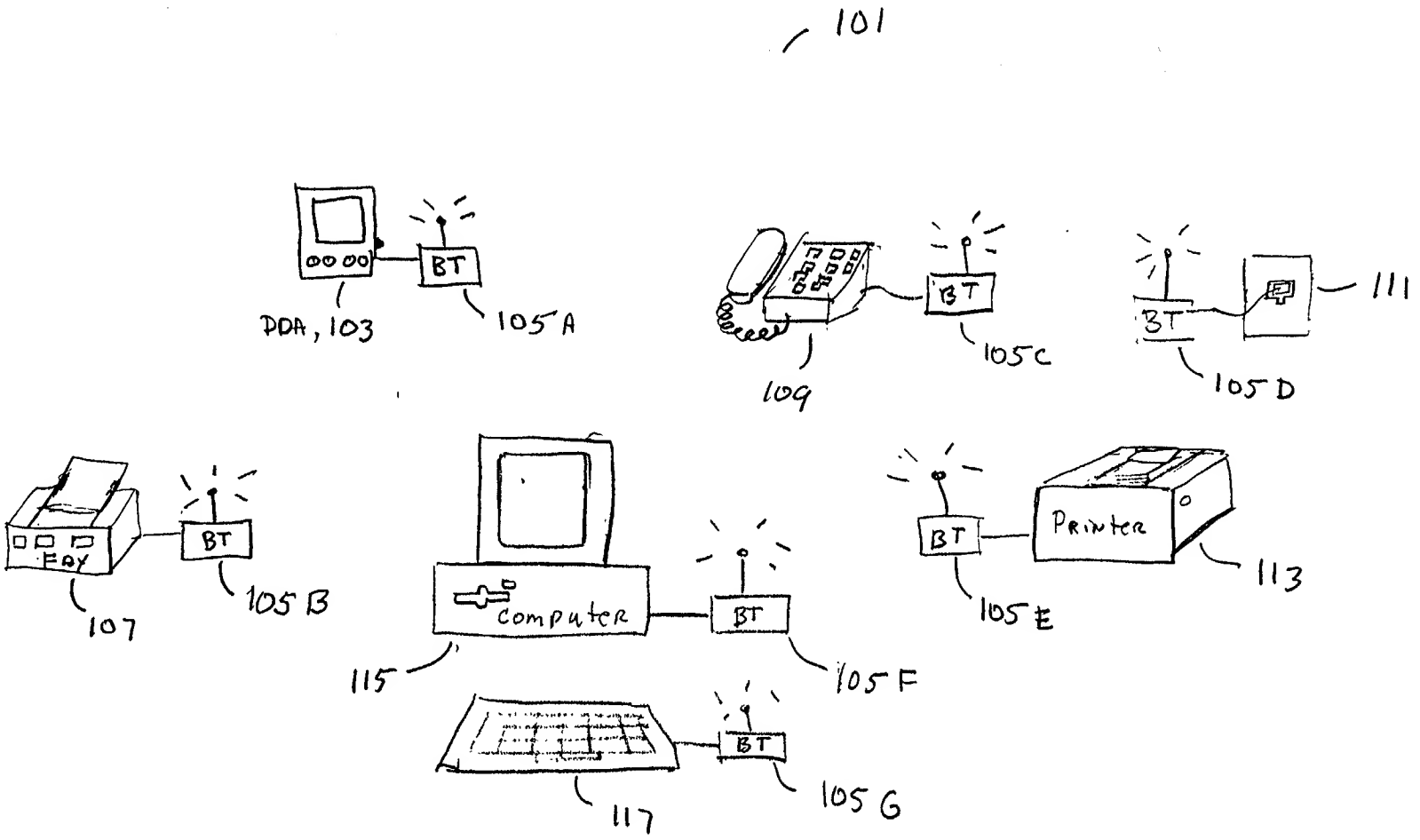


Figure #1

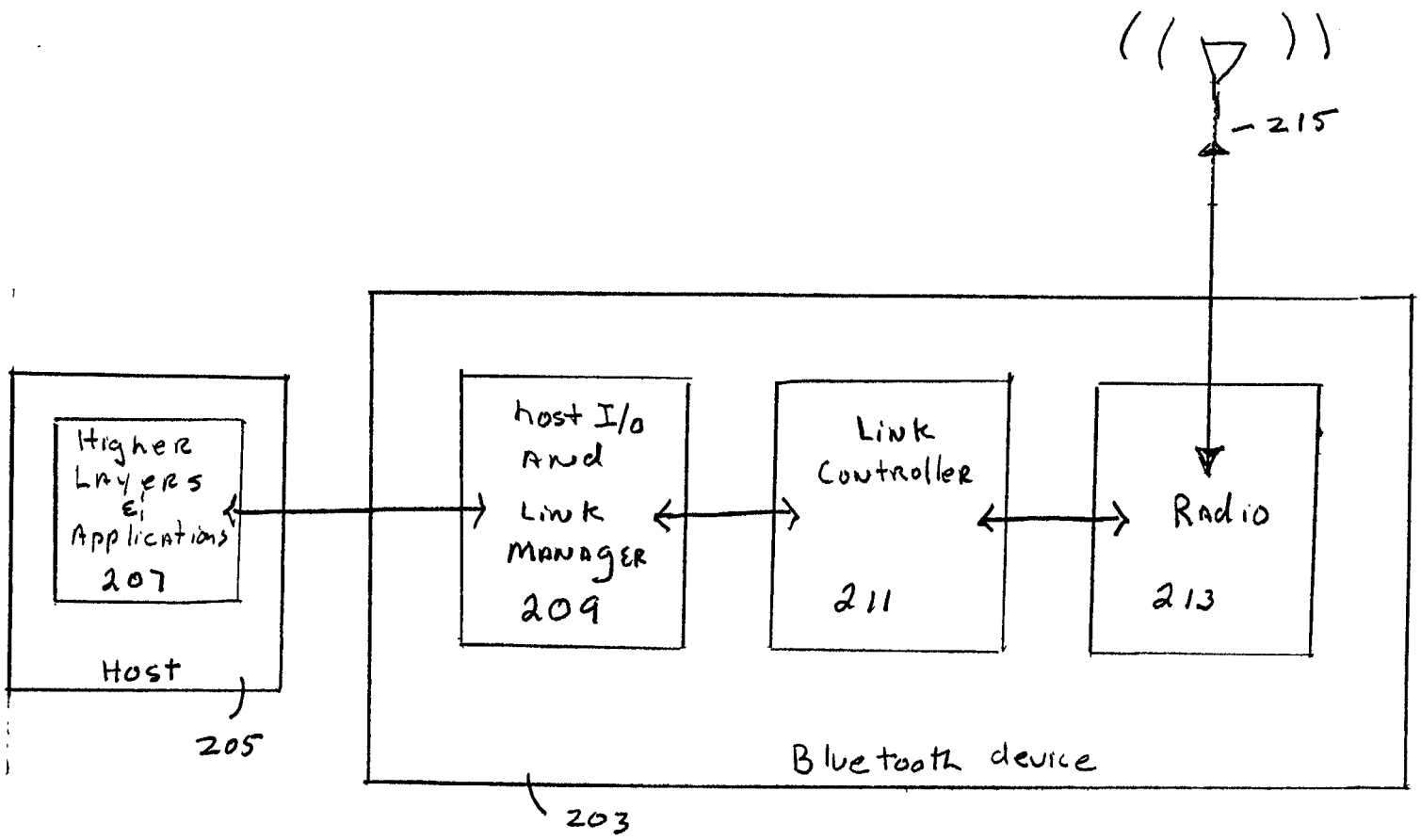


Figure 2A

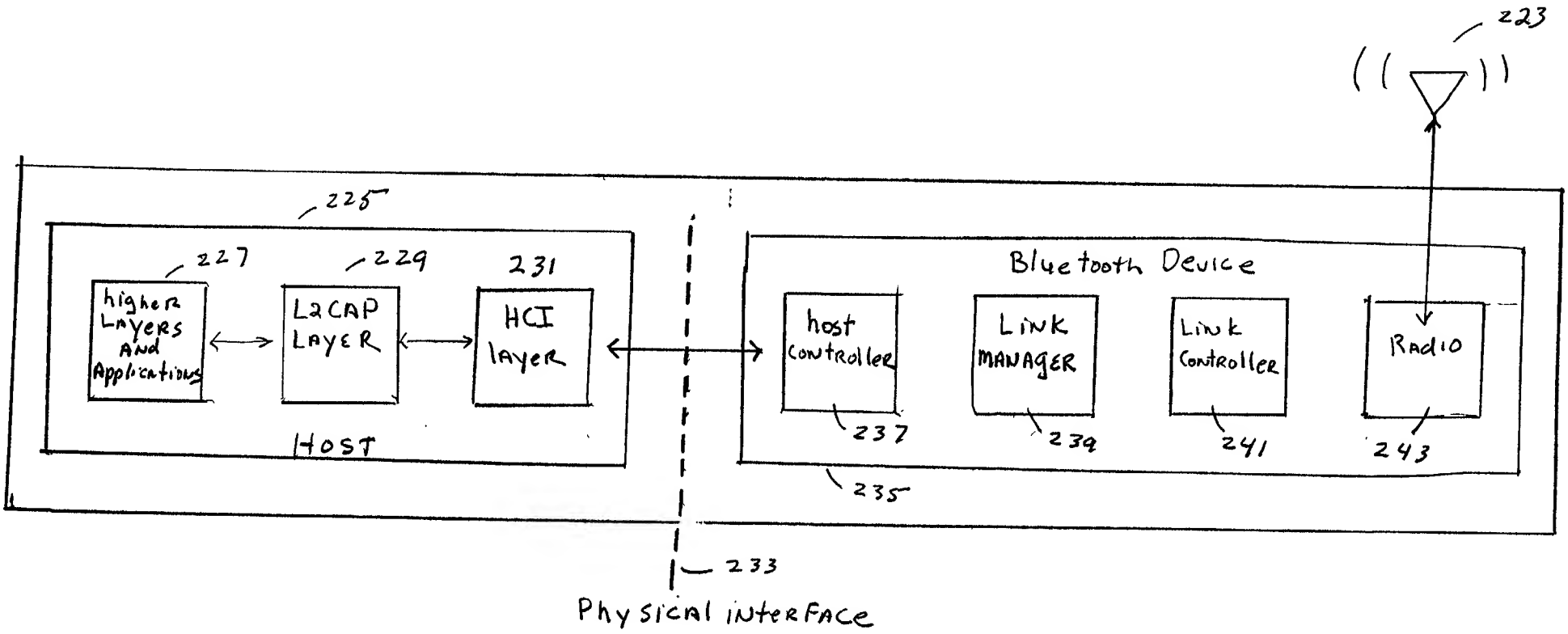


Figure 2B

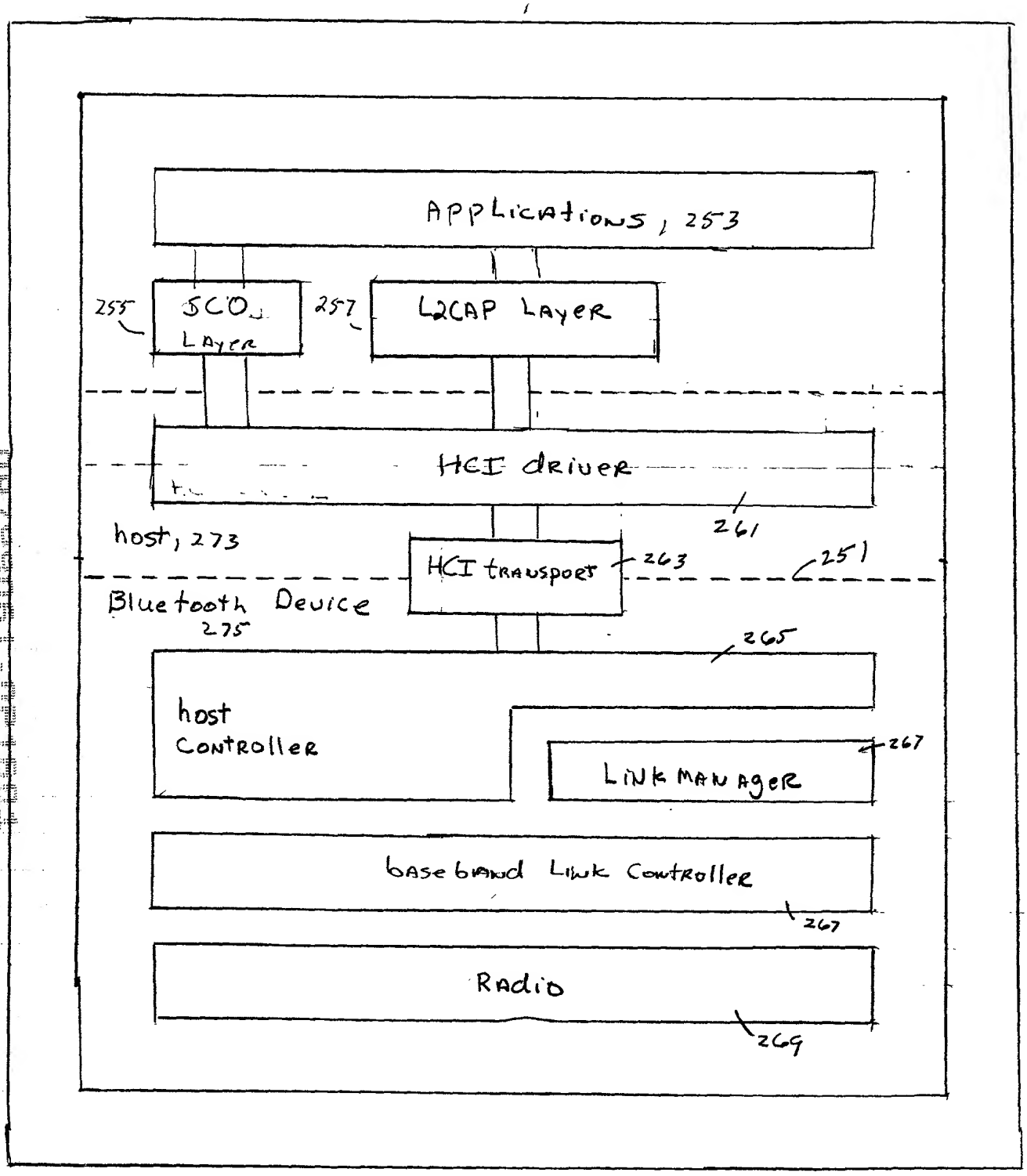

APPLICATIONS, 253
255
SCO LAYER
257
L2CAP LAYER
HCI driver
261
host, 273
HCI transport
263
251
Bluetooth Device
275
265
host
CONTROLLER
267
LINK MANAGER
baseband Link Controller
267
Radio
269

Figure 2C

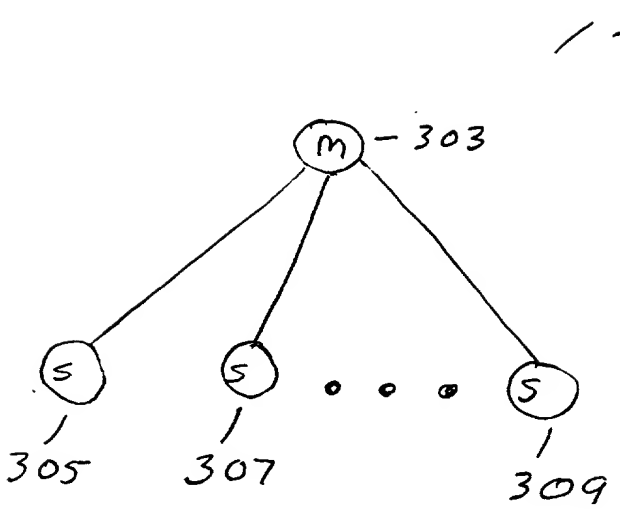


Figure #3

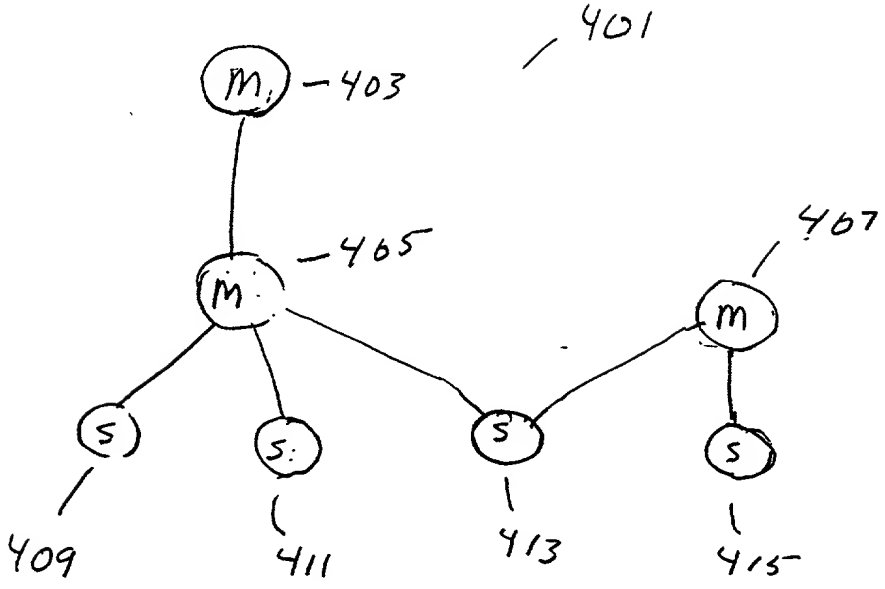


Figure #4

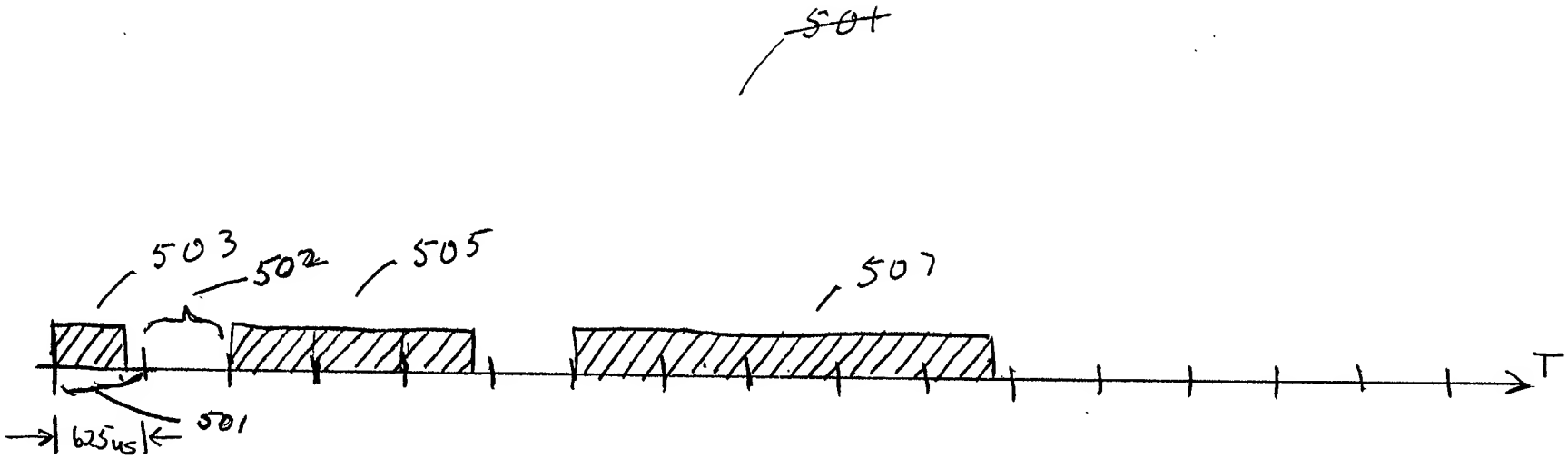


Figure 5

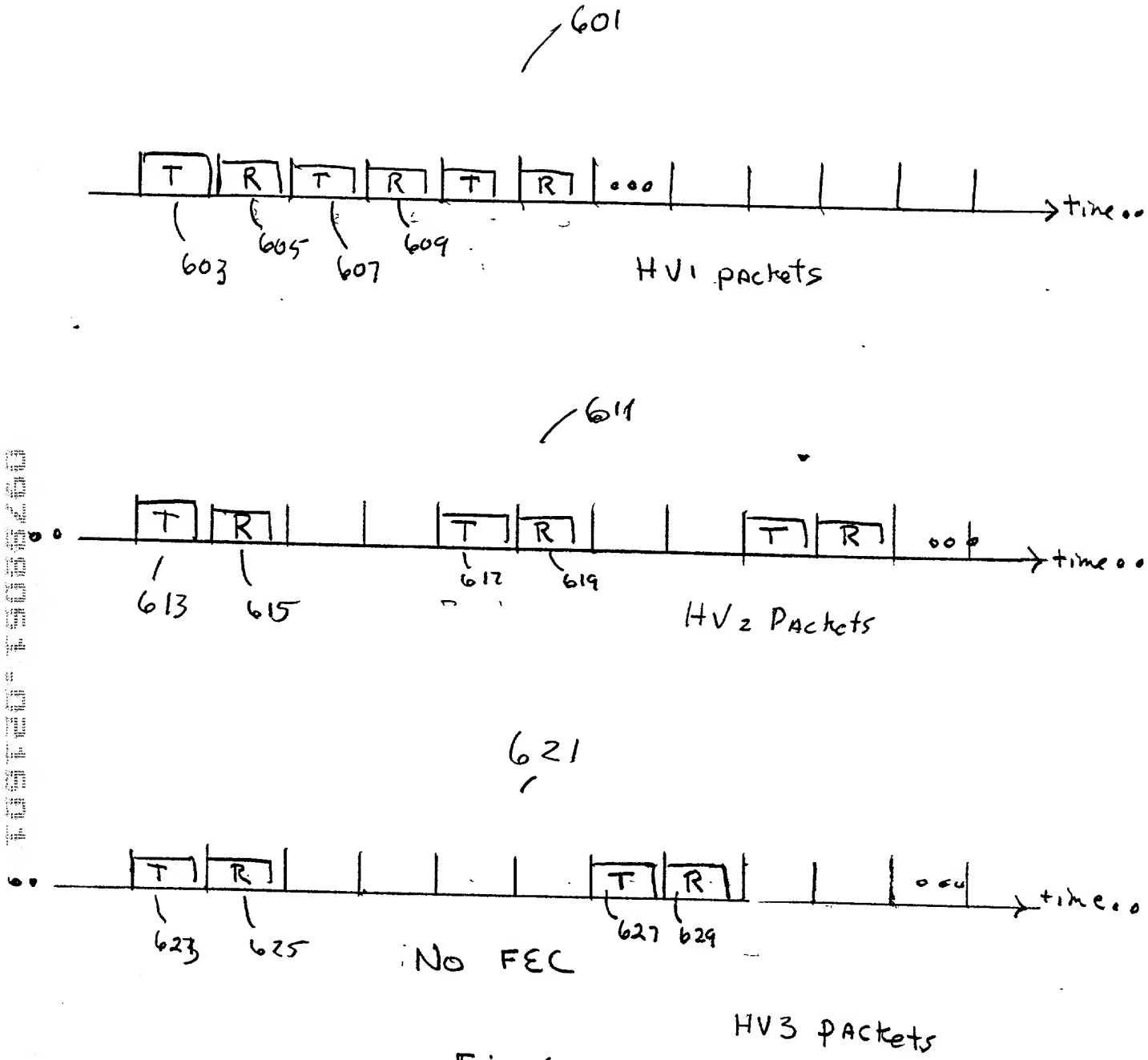

601
T
R
T
R
T
R
time
603
605
607
609
HV1 packets
611
T
R
T
R
T
R
time
613
615
617
619
HV2 Packets
621
T
R
T
R
time
623
625
627
629
No FEC
HV3 packets

Fig 6

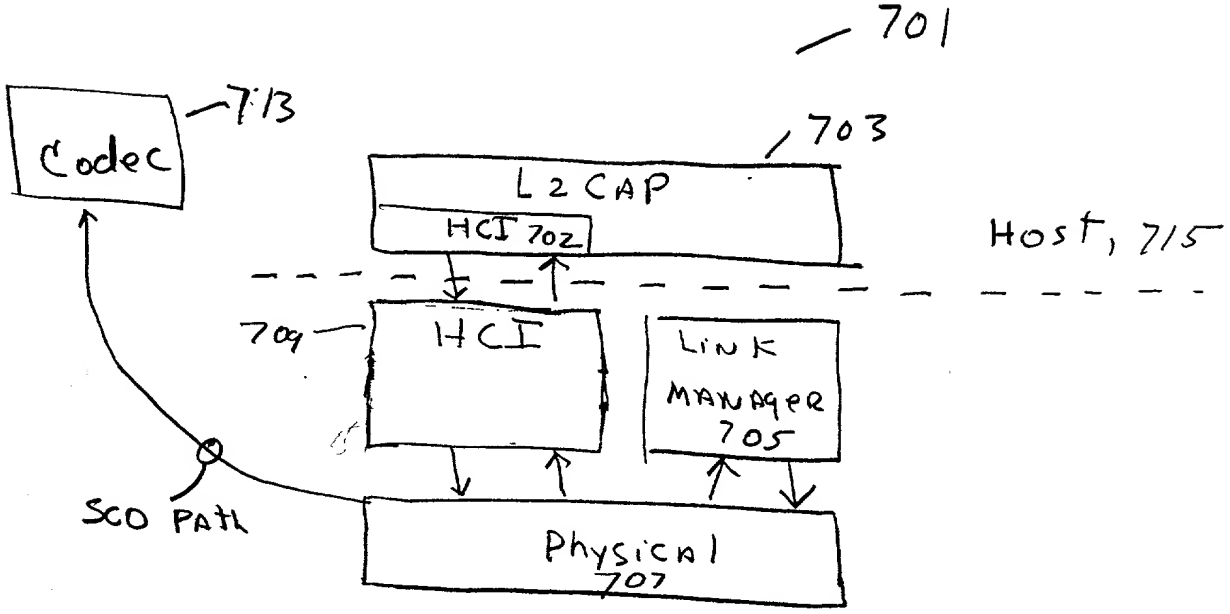

701
Codec
713
703
L2CAP
HCI 702
Host, 715
709
HCI
LINK
MANAGER
705
SCO PATH
Physical
707

Figure #7

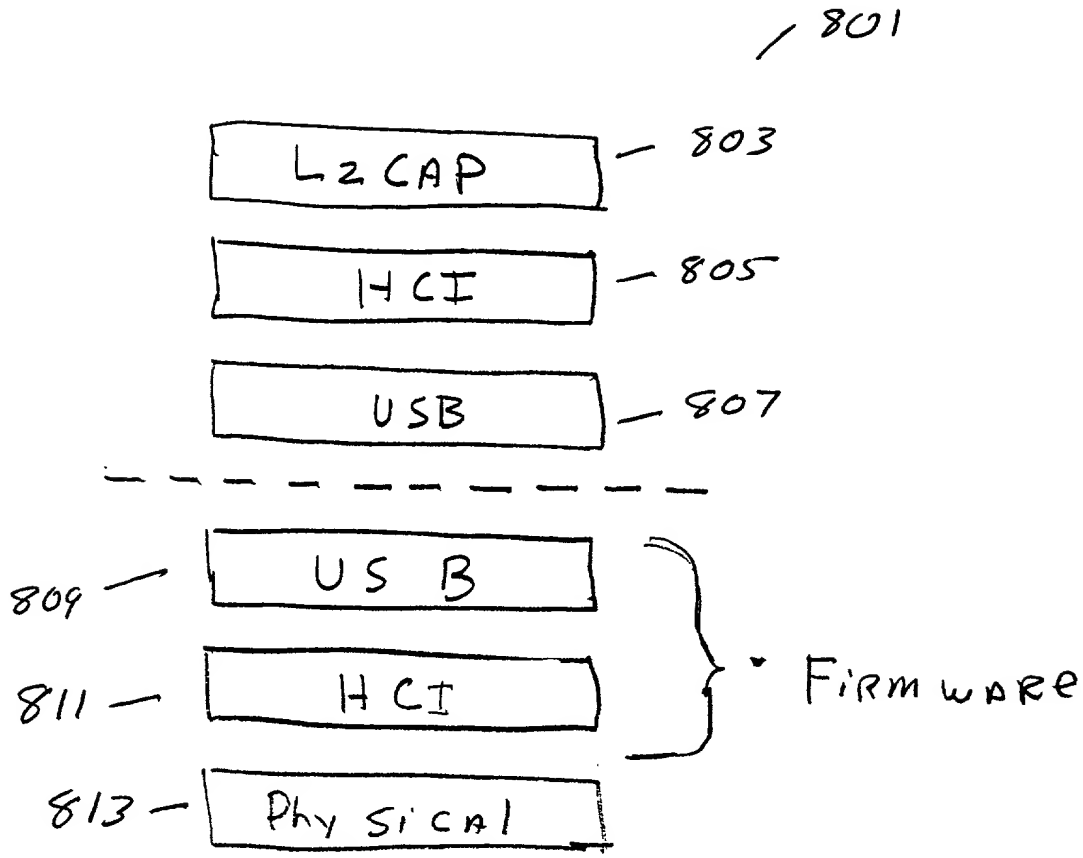

801
L2CAP
803
HCI
805
USB
807
USB
809
HCI
811
Physical
813
Firmware

Figure 8

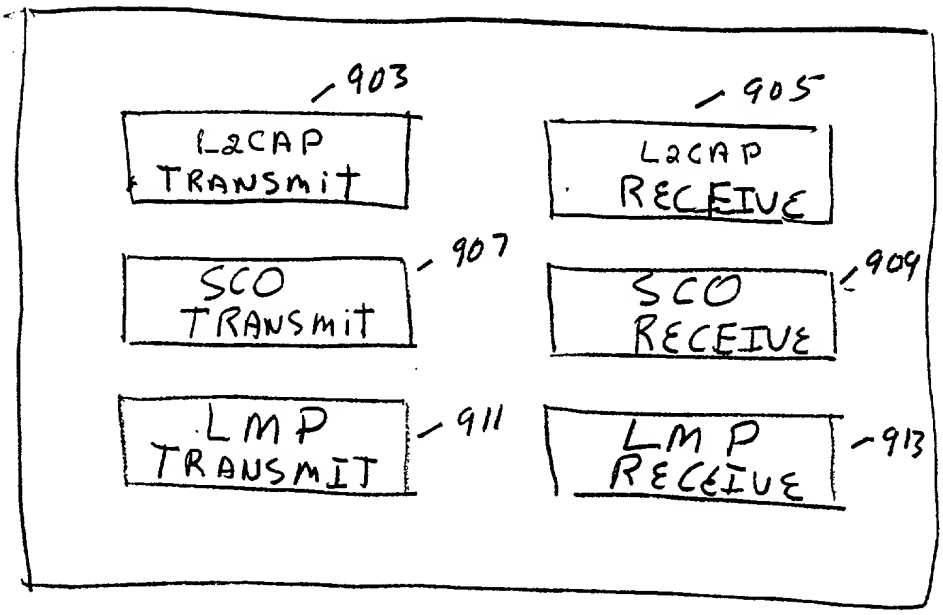

901
903
L2CAP TRANSMIT
905
L2CAP RECEIVE
907
SCO TRANSMIT
909
SCO RECEIVE
911
LMP TRANSMIT
913
LMP RECEIVE

Figure # 9

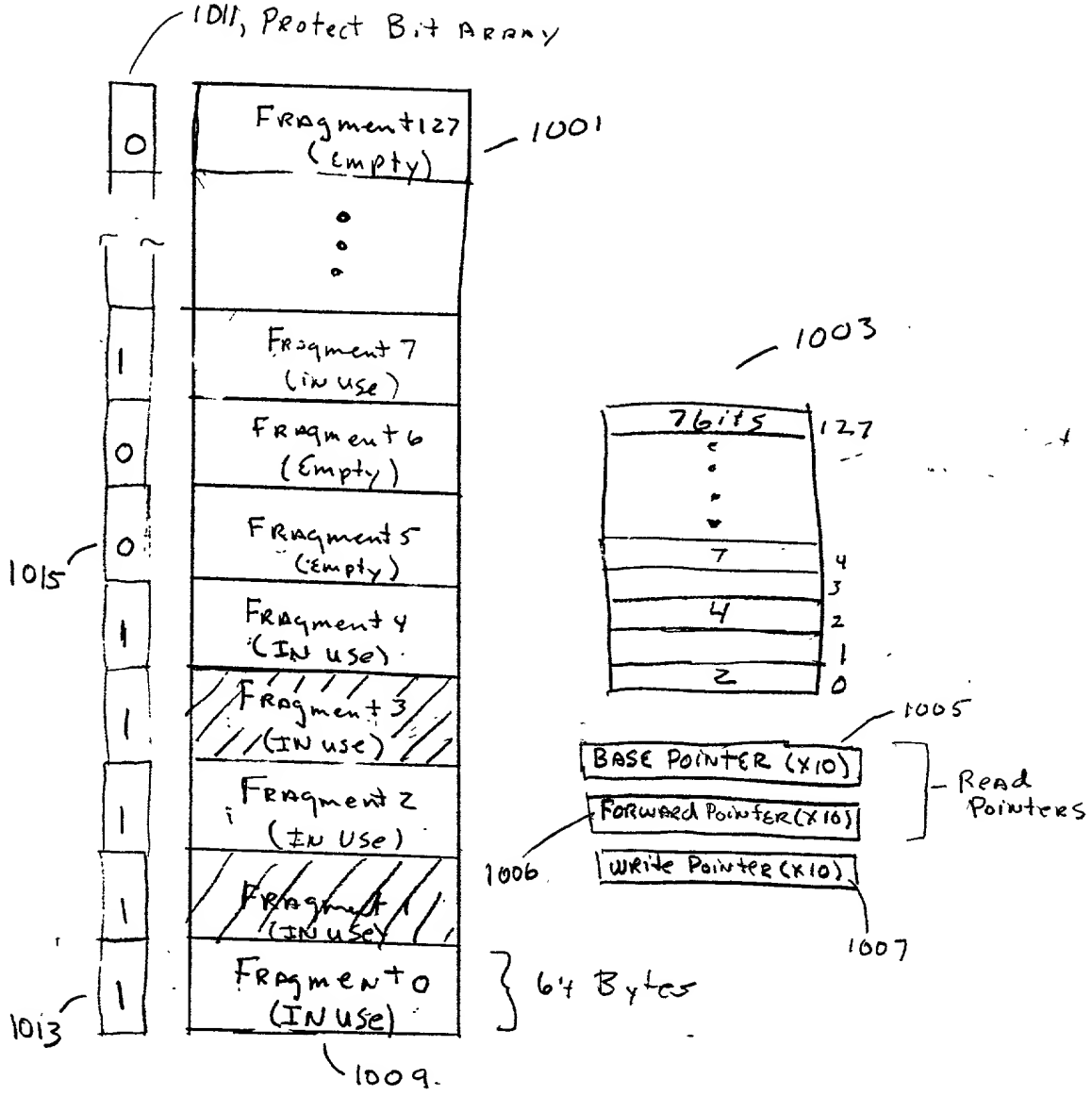

1011, Protect Bit Array
Fragment 127 (Empty)
1001
Fragment 7 (in use)
Fragment 6 (Empty)
Fragment 5 (Empty)
Fragment 4 (IN use)
Fragment 3 (IN use)
Fragment 2 (IN use)
Fragment 1 (IN use)
Fragment 0 (IN use)
1015
1013
1009
64 Bytes
1003
76 bits
127
7
4
3
4
2
1
2
0
1005
BASE POINTER (X10)
FORWARD POINTER (X10)
WRITE POINTER (X10)
Read Pointers
1006
1007

Figure # 10

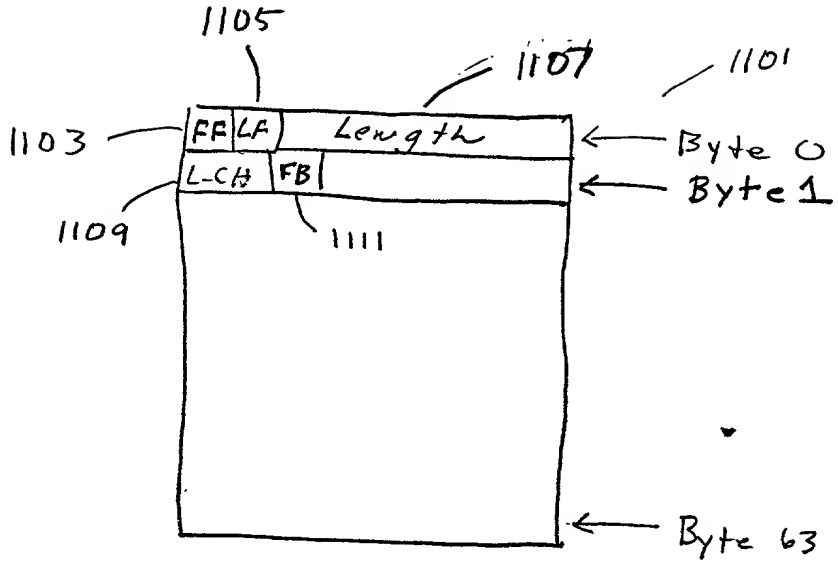

1105
1107
1101
1103
FF
LA
Length
Byte 0
L-CH
FB
Byte 1
1109
1111
Byte 63

Figure # 11

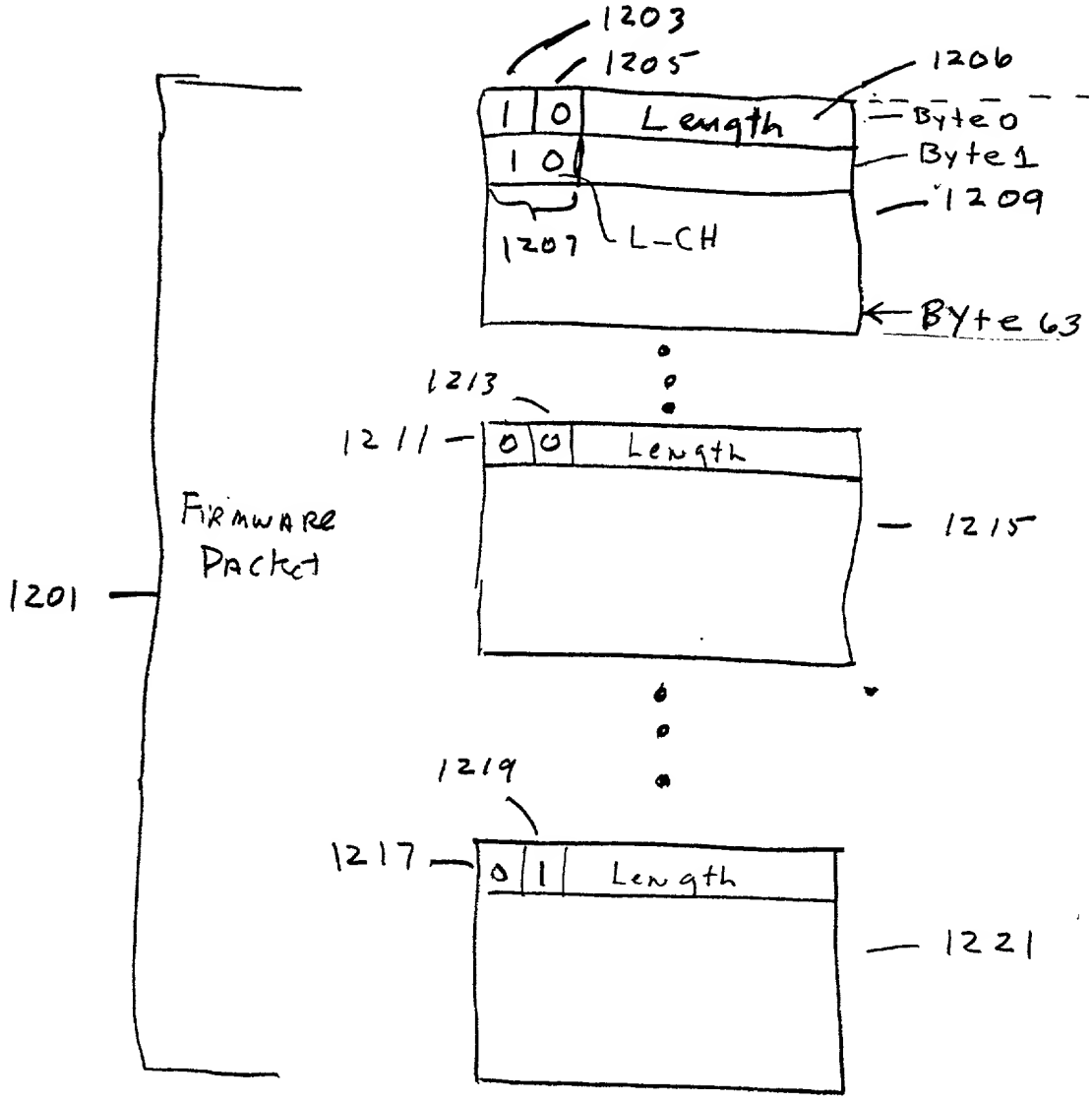

1203
1205
1206
1 0
Length
Byte 0
1 0
Byte 1
1209
1207
L-CH
Byte 63
1213
1211
0 0
Length
1215
Firmware
Packet
1201
1219
1217
0 1
Length
1221

Figure 12

Figure 13

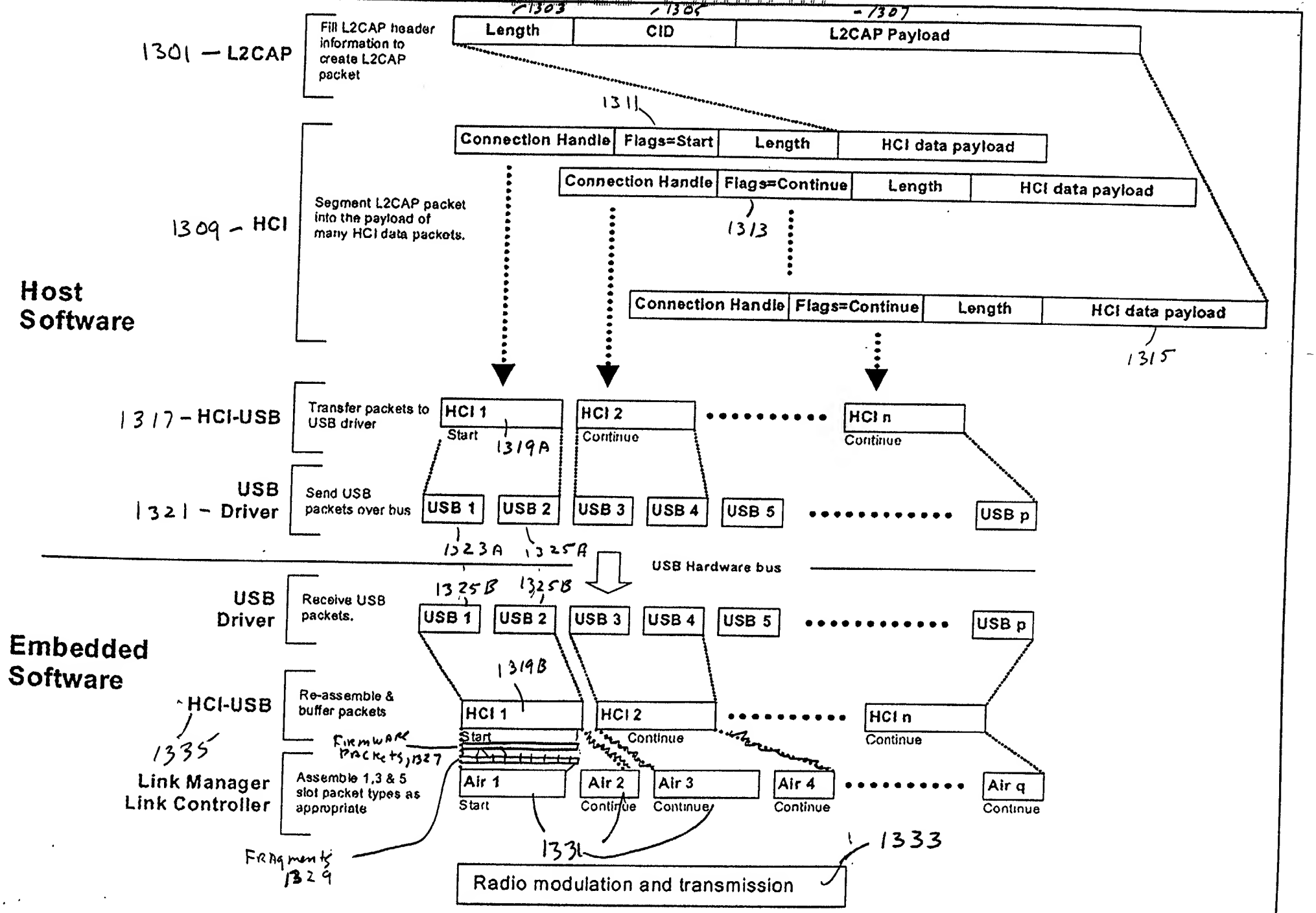
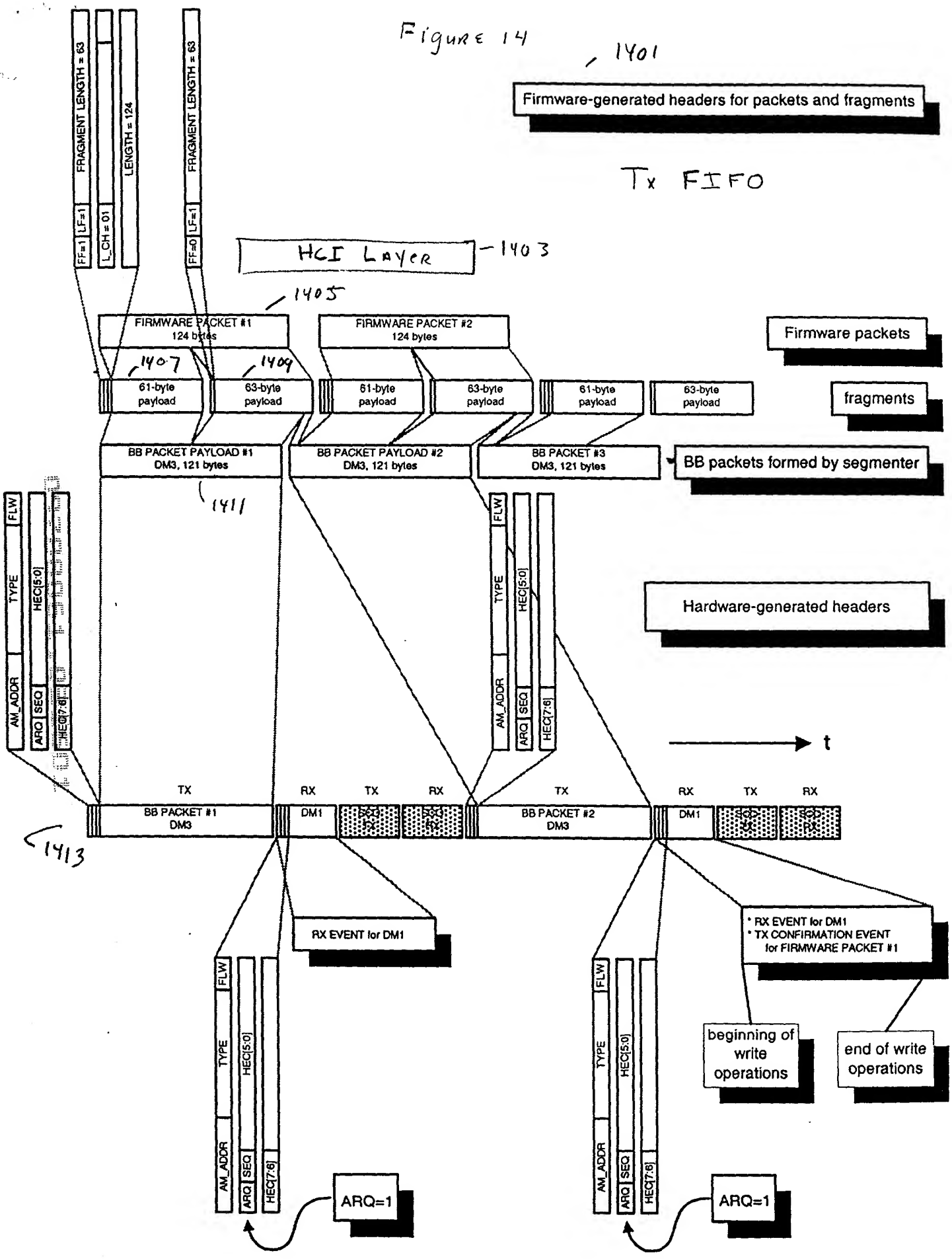

1303
1305
1307
1301 — L2CAP
Fill L2CAP header information to create L2CAP packet
Length
CID
L2CAP Payload
1311
Connection Handle
Flags=Start
Length
HCI data payload
Connection Handle
Flags=Continue
Length
HCI data payload
1309 – HCI
Segment L2CAP packet into the payload of many HCI data packets.
1313
Host Software
Connection Handle
Flags=Continue
Length
HCI data payload
1315
1317 – HCI-USB
Transfer packets to USB driver
HCI 1
Start
1319A
HCI 2
Continue
HCI n
Continue
USB 1321 – Driver
Send USB packets over bus
USB 1
USB 2
USB 3
USB 4
USB 5
USB p
1323A
1325A
USB Hardware bus
1325B
1325B
USB Driver
Receive USB packets.
USB 1
USB 2
USB 3
USB 4
USB 5
USB p
Embedded Software
1319B
HCI-USB
Re-assemble & buffer packets
HCI 1
Start
HCI 2
Continue
HCI n
Continue
1335
Firmware Packets 1327
Link Manager Link Controller
Assemble 1,3 & 5 slot packet types as appropriate
Air 1
Start
Air 2
Continue
Air 3
Continue
Air 4
Continue
Air q
Continue
Fragments 1329
1331
1333
Radio modulation and transmission

Figure 14


1401
Firmware-generated headers for packets and fragments
Tx FIFO
HCI Layer
1403
1405
FIRMWARE PACKET #1
124 bytes
FIRMWARE PACKET #2
124 bytes
Firmware packets
1407
1409
61-byte payload
63-byte payload
61-byte payload
63-byte payload
61-byte payload
63-byte payload
fragments
BB PACKET PAYLOAD #1
DM3, 121 bytes
BB PACKET PAYLOAD #2
DM3, 121 bytes
BB PACKET #3
DM3, 121 bytes
BB packets formed by segmenter
1411
Hardware-generated headers
FRAGMENT LENGTH = 63
FF=1
LF=1
L_CH = 01
LENGTH = 124
FRAGMENT LENGTH = 63
FF=0
LF=1
FLW
TYPE
HEC[5:0]
AM_ADDR
ARQ
SEQ
HEC[7:6]
t
TX
RX
TX
RX
TX
RX
TX
RX
BB PACKET #1
DM3
DM1
BB PACKET #2
DM3
DM1
1413
RX EVENT for DM1
* RX EVENT for DM1
* TX CONFIRMATION EVENT
for FIRMWARE PACKET #1
beginning of write operations
end of write operations
ARQ=1
ARQ=1

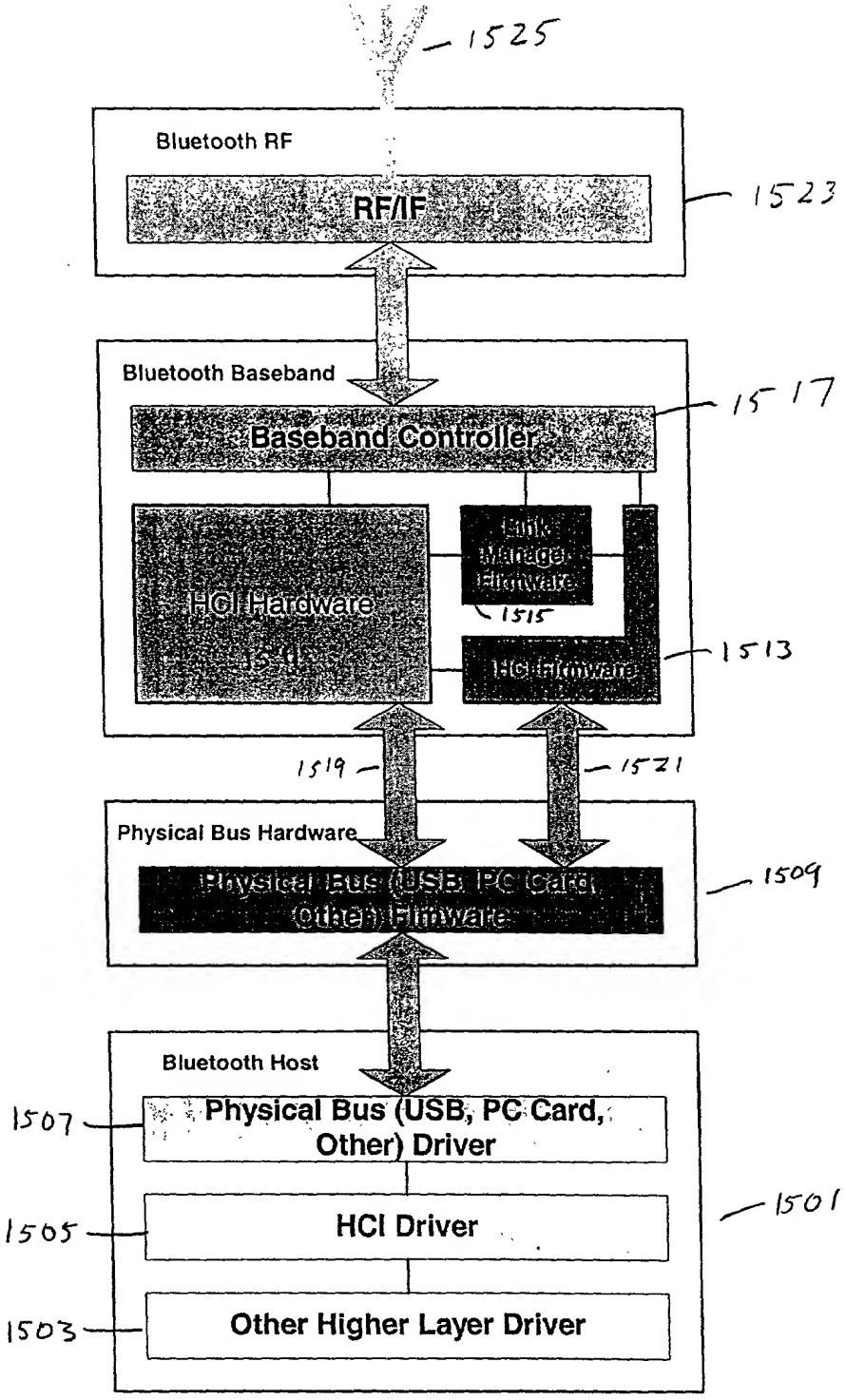

1525
Bluetooth RF
RF/IF
1523
Bluetooth Baseband
1517
Baseband Controller
HCI Hardware
1511
Link Manage Firmware
1515
HCI Firmware
1513
1519
1521
Physical Bus Hardware
Physical Bus (USB, PC Card, Other) Firmware
1509
Bluetooth Host
1507
Physical Bus (USB, PC Card, Other) Driver
1505
HCI Driver
1503
Other Higher Layer Driver
1501

Figure 15

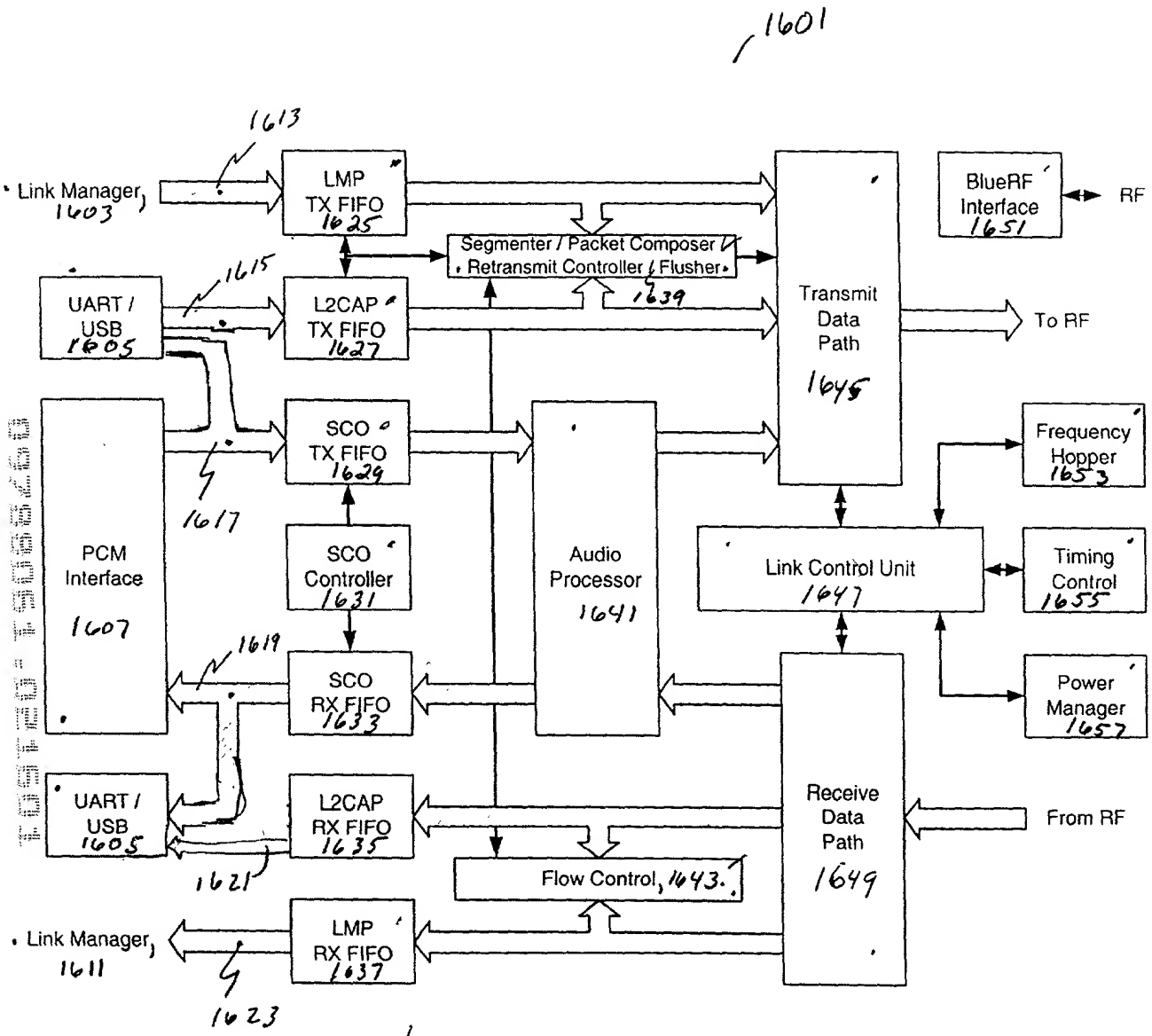

1601
1613
Link Manager
1603
LMP
TX FIFO
1625
Segmenter / Packet Composer
Retransmit Controller / Flusher
1639
BlueRF
Interface
1651
RF
1615
UART /
USB
1605
L2CAP
TX FIFO
1627
Transmit
Data
Path
1645
To RF
SCO
TX FIFO
1629
Frequency
Hopper
1653
1617
PCM
Interface
1607
SCO
Controller
1631
Audio
Processor
1641
Link Control Unit
1647
Timing
Control
1655
1619
SCO
RX FIFO
1633
Power
Manager
1657
UART /
USB
1605
L2CAP
RX FIFO
1635
Receive
Data
Path
1649
From RF
1621
Flow Control
1643
Link Manager
1611
LMP
RX FIFO
1637
1623

FIGURE 16

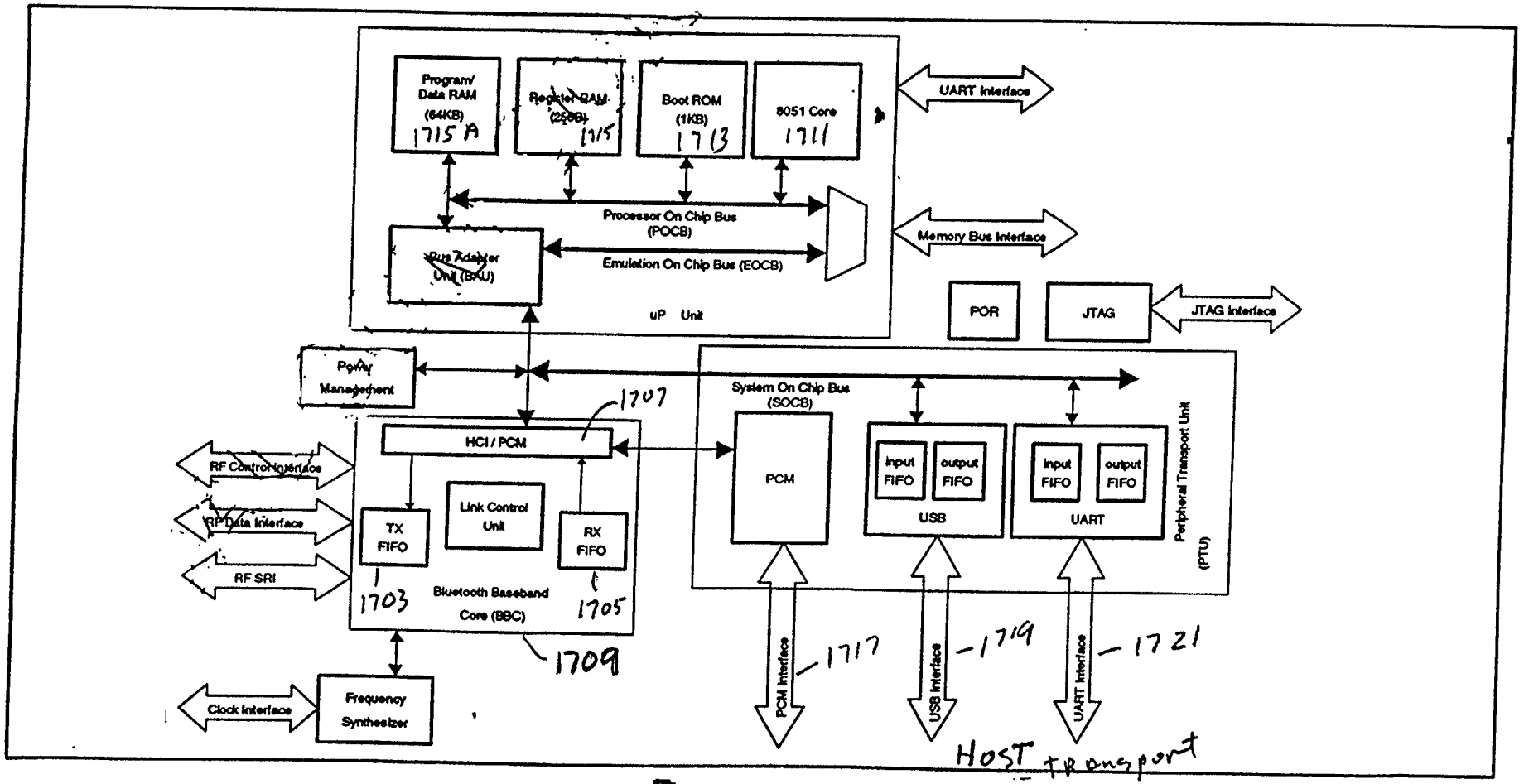


Figure 17

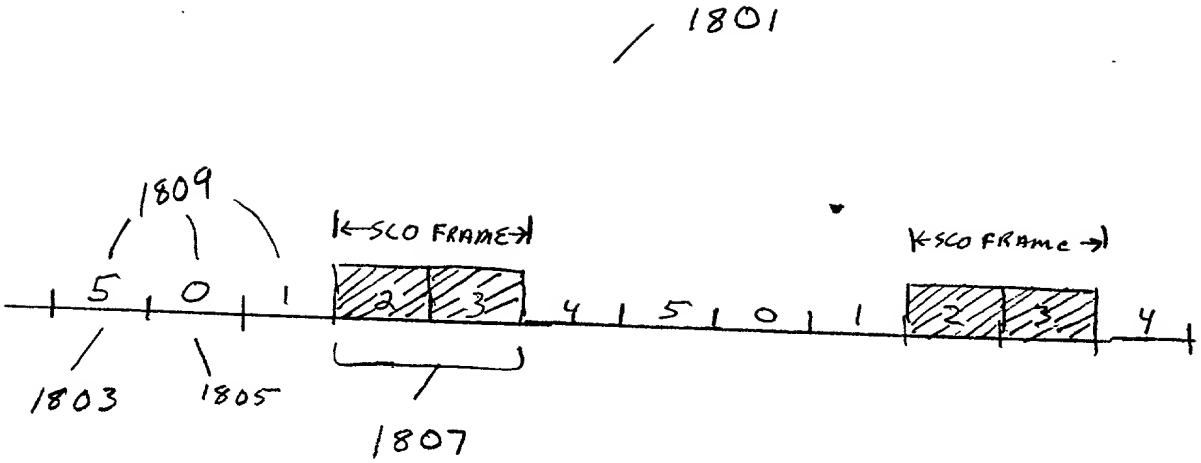


Figure 18

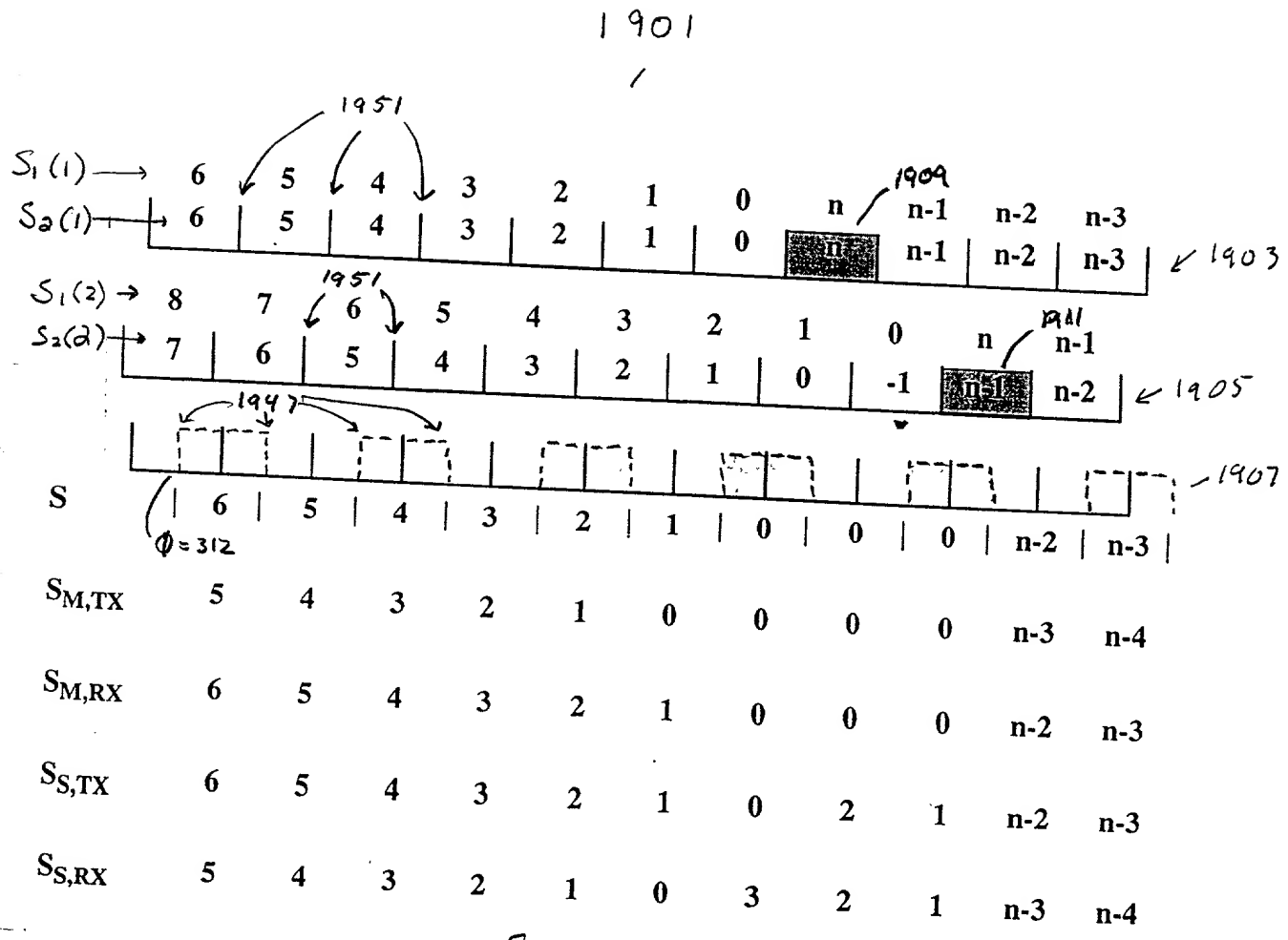


Figure 19A

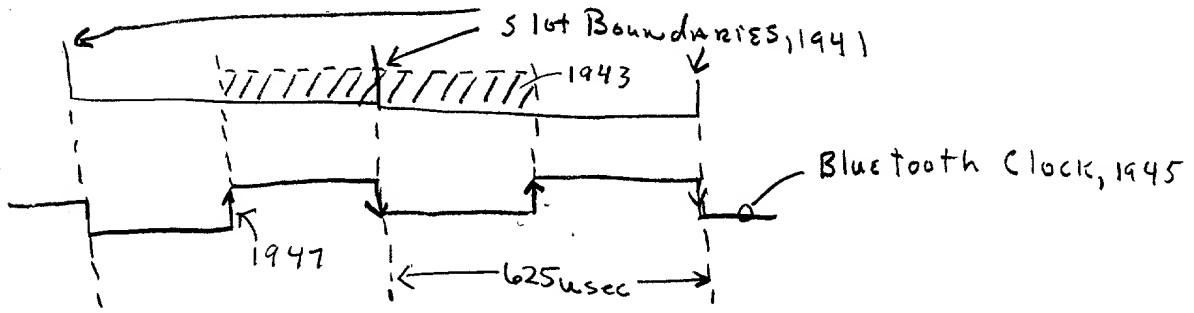


Figure 19B

2001

Table 1. Packet Type Priority

Range Label	Min Bytes in Buffer	Max Bytes in Buffer	1st Choice	2nd Choice	3rd Choice	4th Choice	5th Choice	6th Choice
a	0	0	NULL	NULL	NULL	NULL	NULL	NULL
b	1	17	DM1	DH1	DM3	DH3	DM5	DH5
c	18	27	DH1	DM3	DH3	DM5	DH5	DM1
d	28	121	DM3	DH3	DM5	DH5	DH1	DM1
e	122	183	DH3	DM5	DH5	DM3	DH1	DM1
f	184	224	DM5	DH5	DH3	DM3	DH1	DM1
g	225	339	DH5	DM5	DH3	DM3	DH1	DM1
h	339		DH5	DM5	DH3	DM3	DH1	DM1

Figure 20

Figure 1. Example of a Fragment Chooser for 16 fragments, N = 4

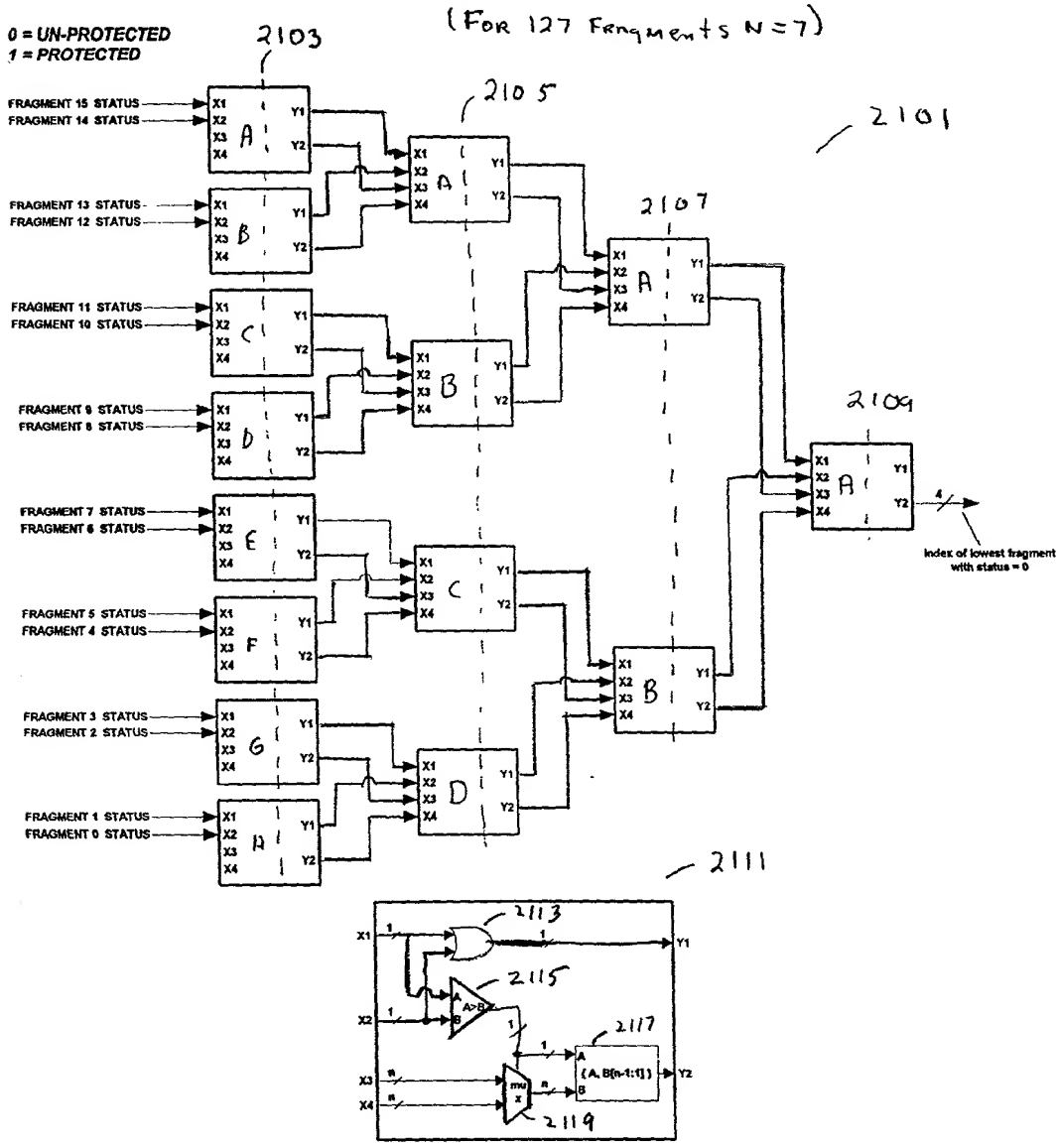


Figure 21

Figure 22Circuit to calculate CLK mod T, where CLK is 27 bits and T is 8 bits.

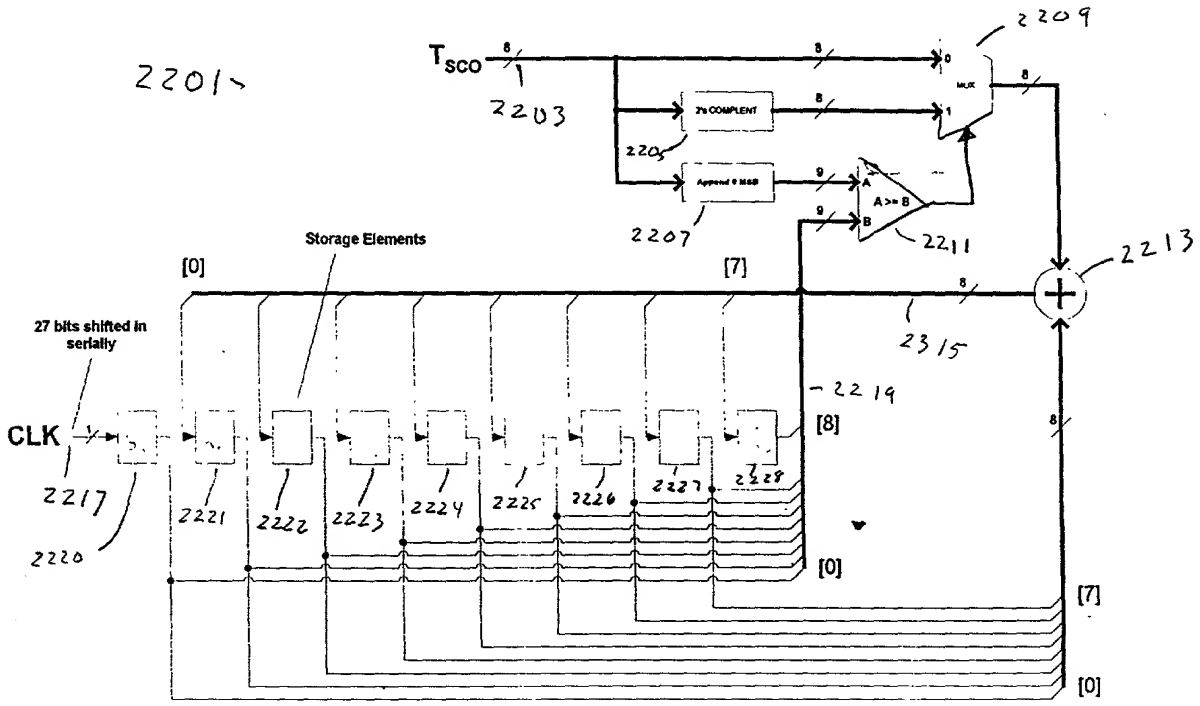


FIGURE 22

Figure 3. Example calculation: 115307261 mod 135

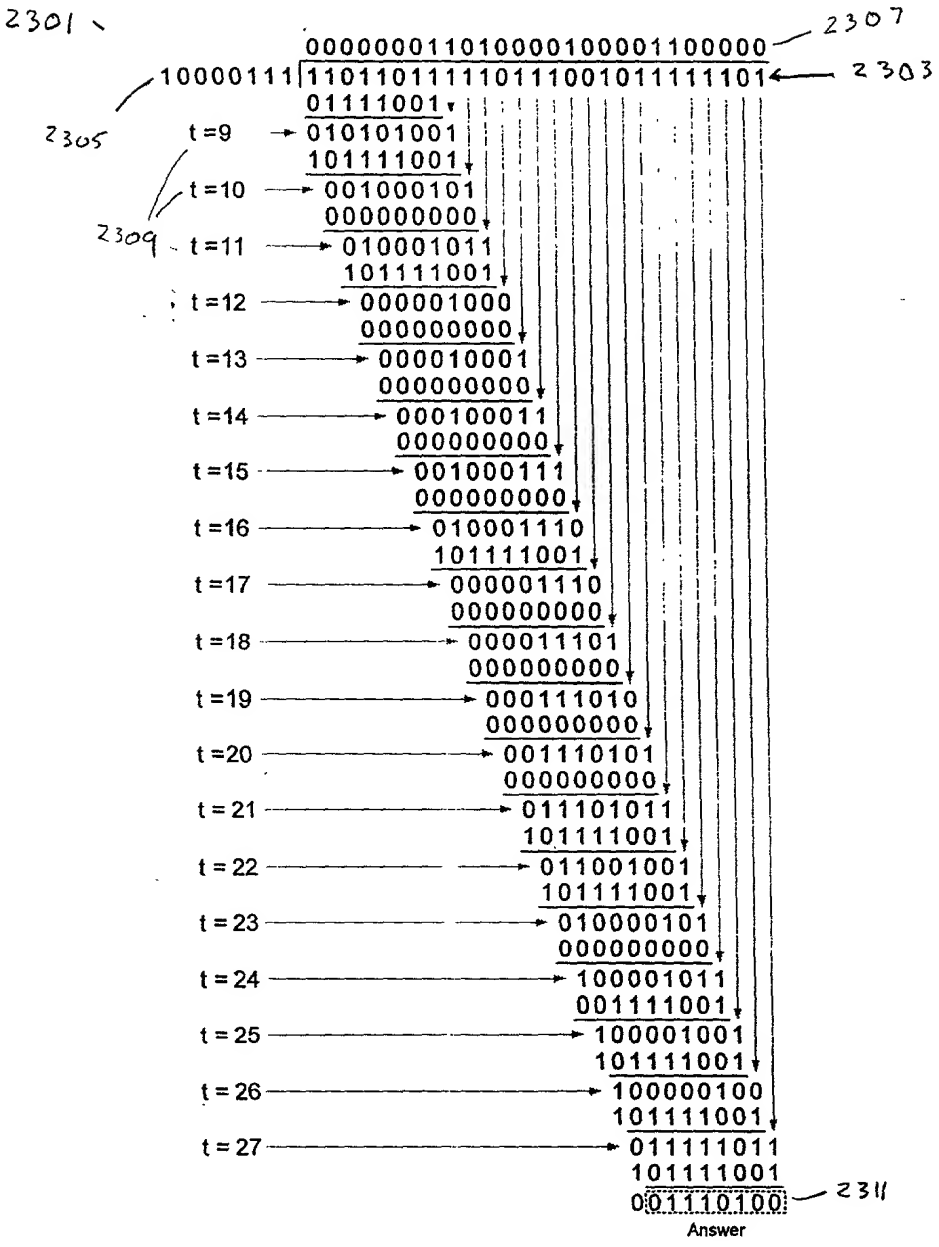


Figure 23

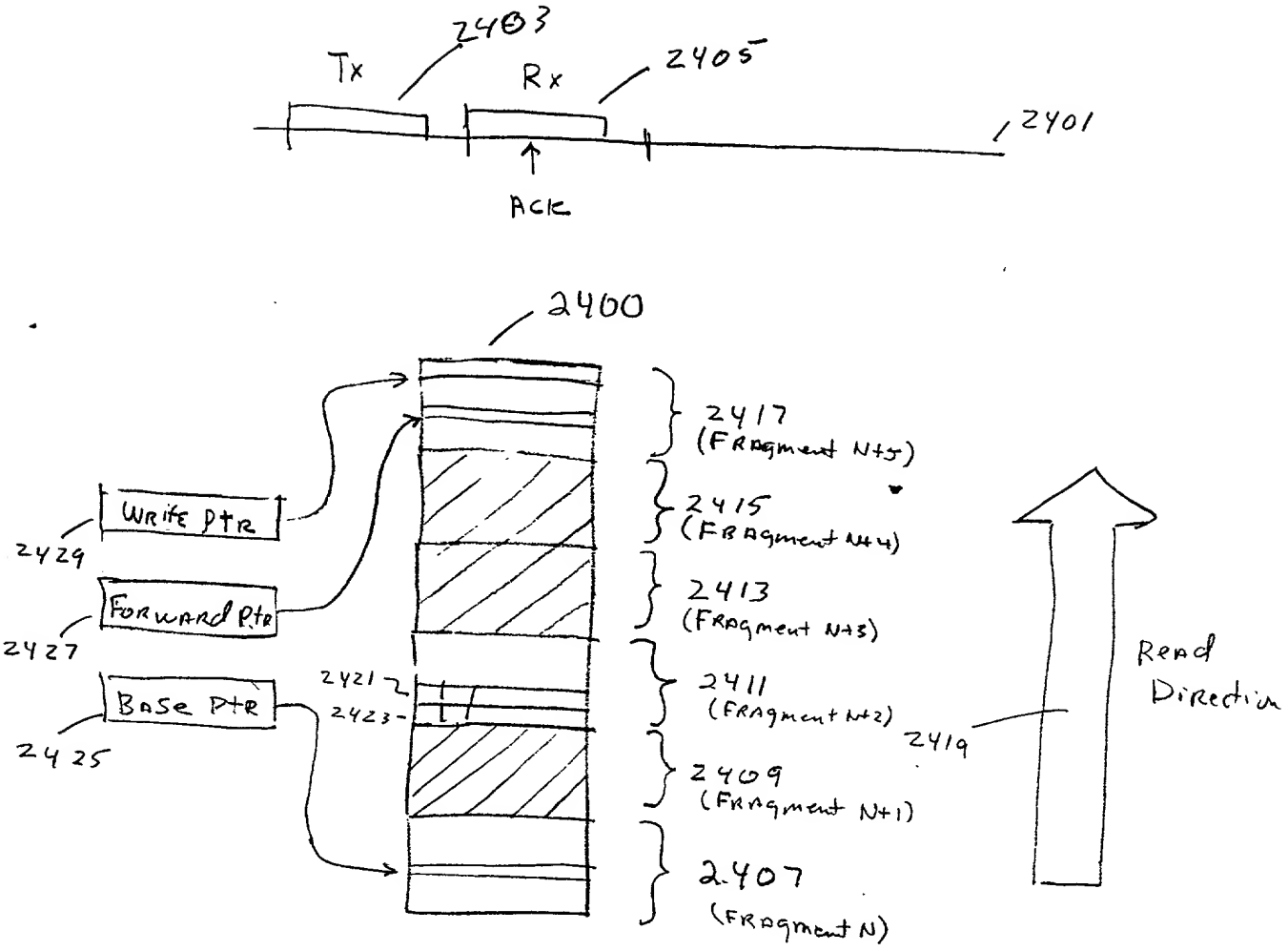

2403
Tx
Rx
2405
2401
ACK
2400
2417
(Fragment N+3)
2415
(Fragment N+4)
2413
(Fragment N+3)
2411
(Fragment N+2)
2409
(Fragment N+1)
2407
(Fragment N)
Write Ptr
2429
Forward Ptr
2427
Base Ptr
2425
2421
2423
2419
Read
Direction

Figure 24

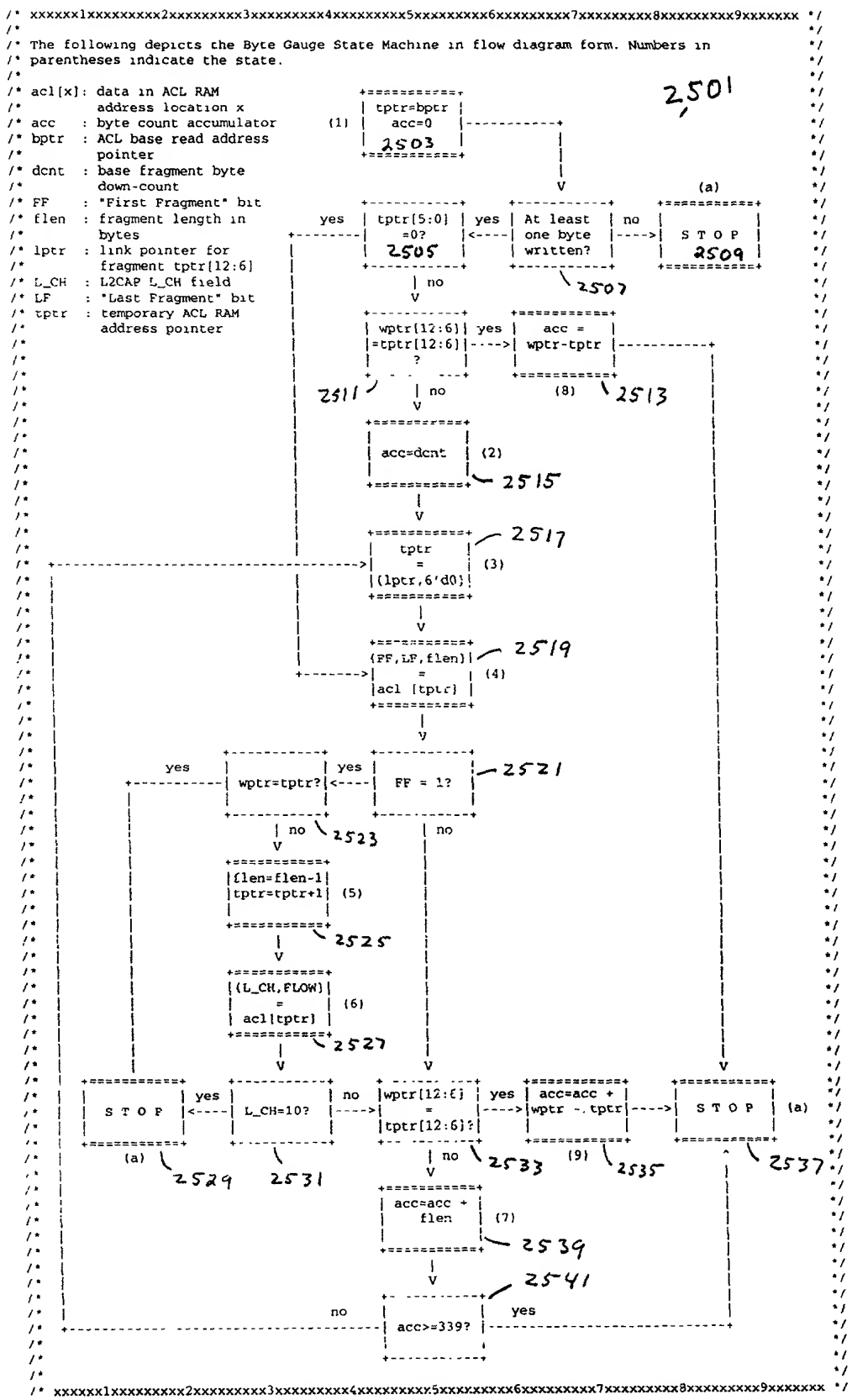
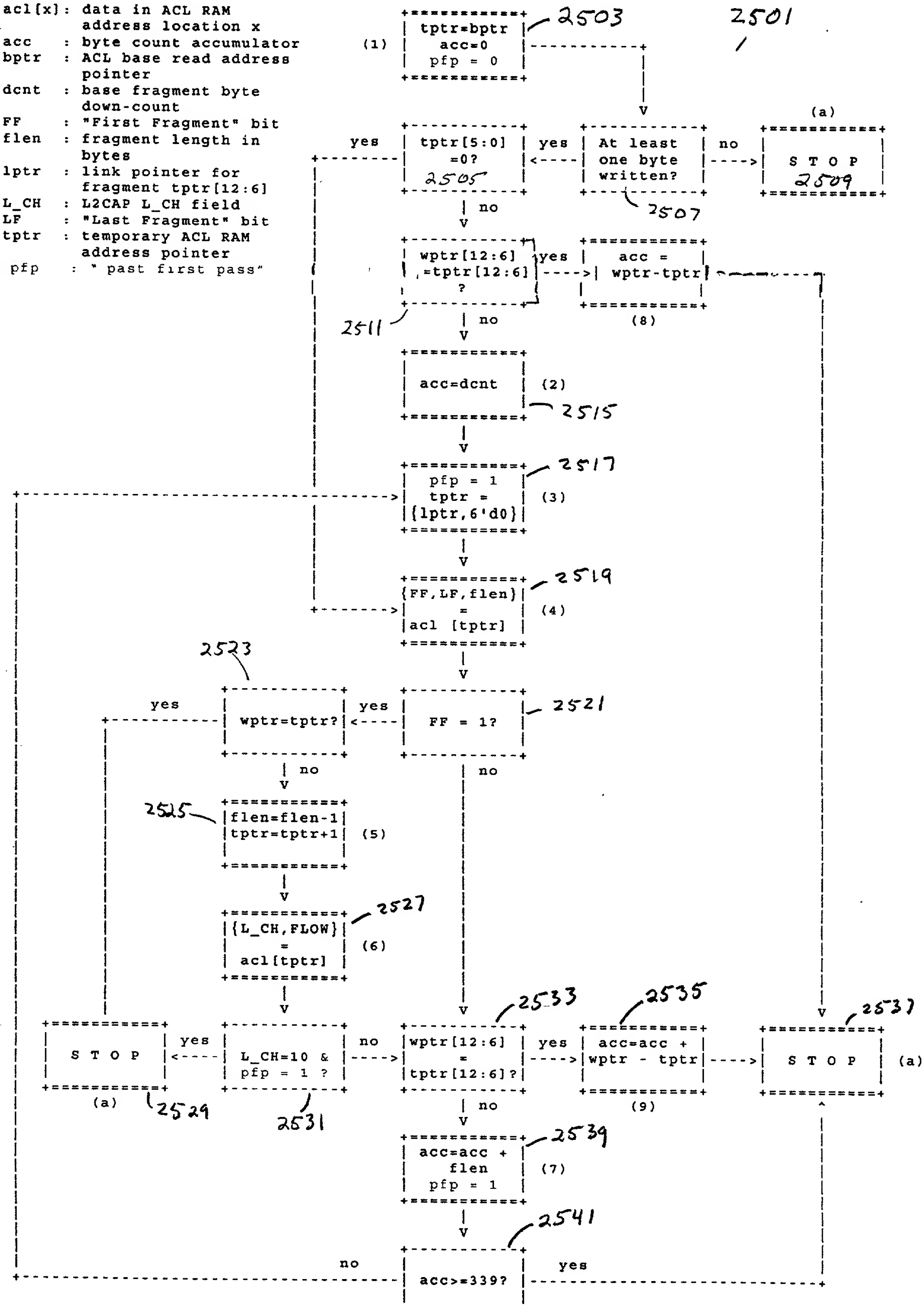

/* xxxxxx1xxxxxxxxx2xxxxxxxxx3xxxxxxxxx4xxxxxxxxx5xxxxxxxxx6xxxxxxxxx7xxxxxxxxx8xxxxxxxxx9xxxxxxx */
/* The following depicts the Byte Gauge State Machine in flow diagram form. Numbers in
/* parentheses indicate the state.
/* acl[x]: data in ACL RAM
/* address location x
/* acc : byte count accumulator
/* bptr : ACL base read address pointer
/* dcnt : base fragment byte down-count
/* FF : "First Fragment" bit
/* flen : fragment length in bytes
/* lptr : link pointer for fragment tptr[12:6]
/* L_CH : L2CAP L_CH field
/* LF : "Last Fragment" bit
/* tptr : temporary ACL RAM address pointer
2501
tptr=bptr
acc=0
(1)
2503
tptr[5:0] =0?
2505
At least one byte written?
2507
STOP
2509
(a)
wptr[12:6] =tptr[12:6] ?
2511
acc = wptr-tptr
(8)
2513
acc=dcnt
(2)
2515
tptr = (lptr,6'd0)
(3)
2517
{FF,LF,flen} = acl [tptr]
(4)
2519
FF = 1?
2521
wptr=tptr?
2523
flen=flen-1
tptr=tptr+1
(5)
2525
{L_CH,FLOW} = acl[tptr]
(6)
2527
STOP
(a)
2529
L_CH=10?
2531
wptr[12:6] =tptr[12:6]?
2533
acc=acc + wptr - tptr
(9)
2535
STOP
(a)
2537
acc=acc + flen
(7)
2539
acc>=339?
2541
yes
no

Figure 25

```
/* xxxxxx1xxxxxxxxx2xxxxxxxxx3xxxxxxxxx4xxxxxxxxx5xxxxxxxxx6xxxxxxxxx7xxxxxxxxx8xxxxxxxxx9xxxxxxx */
/*                                                                                              */
/* The following depicts the Byte Gauge State Machine in flow diagram form. Numbers in          */
/* parentheses indicate the state.                                                              */
/*                                                                                              */
/* acl[x]: data in ACL RAM
/*         address location x
/* acc   : byte count accumulator
/* bptr  : ACL base read address
/*         pointer
/* dcnt  : base fragment byte
/*         down-count
/* FF    : "First Fragment" bit
/* flen  : fragment length in
/*         bytes
/* lptr  : link pointer for
/*         fragment tptr[12:6]
/* L_CH  : L2CAP L_CH field
/* LF    : "Last Fragment" bit
/* tptr  : temporary ACL RAM
/*         address pointer
/* pfp   : " past first pass"
```




```
/* xxxxxx1xxxxxxxxx2xxxxxxxxx3xxxxxxxxx4xxxxxxxxx5xxxxxxxxx6xxxxxxxxx7xxxxxxxxx8xxxxxxxxx9xxxxxxx */
```

Figure 25

L2CAP PACKET FLUSH STATE MACHINE

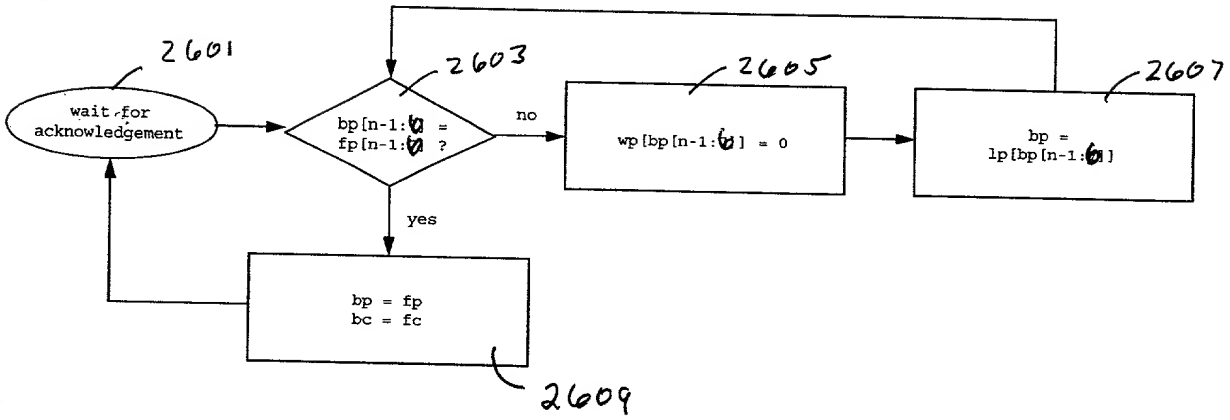
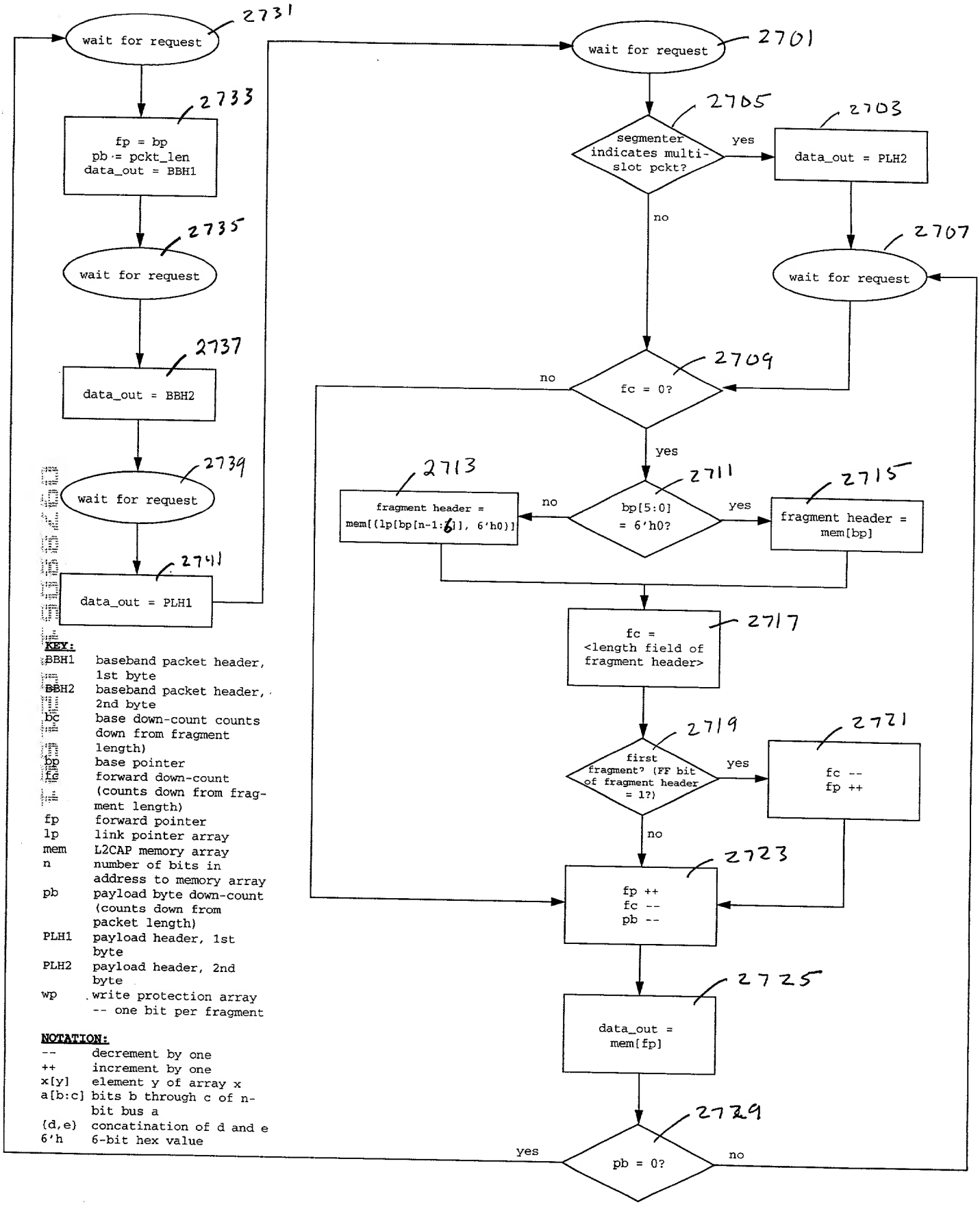


Figure 26

L2CAP PACKET TRANSMIT STATE MACHINE



KEY:

BBH1	baseband packet header, 1st byte
BBH2	baseband packet header, 2nd byte
bc	base down-count counts down from fragment length)
bp	base pointer
fc	forward down-count (counts down from fragment length)
fp	forward pointer
lp	link pointer array
mem	L2CAP memory array
n	number of bits in address to memory array
pb	payload byte down-count (counts down from packet length)
PLH1	payload header, 1st byte
PLH2	payload header, 2nd byte
wp	write protection array -- one bit per fragment

NOTATION:

--	decrement by one
++	increment by one
x[y]	element y of array x
a[b:c]	bits b through c of n-bit bus a
{d,e}	concatination of d and e
6'h	6-bit hex value

Figure 27